WHAT IS CLAIMED IS:

1. A clock and data recovery circuit comprising:

a phase synchronization loop including an oscillator, the oscillation frequency of which is variably controlled, said phase synchronization loop performing phase-synchronization of a clock signal output from said oscillator with an input data signal;

a discriminator circuit, responsive to a clock signal for discrimination, for discriminating said input data signal and outputting the discriminated signal;

a phase detector circuit for detecting the phase difference between an output data signal, discriminated and output by said discriminator circuit, and said input data signal; and

a phase shift circuit for shifting the phase of the clock signal, output from said oscillator, based on a comparison result output from said phase detector circuit;

the clock signal, output from said phase shift circuit, being supplied as said clock signal for discrimination to said discriminator circuit.

2. A clock and data recovery circuit comprising:

a first feedback loop at least including a first phase detector circuit for detecting the phase difference between a clock signal and a received data signal;

a second feedback loop including a discriminator circuit supplied with said received data signal, and a second phase detector circuit for detecting the phase difference between the data signal, discriminated

and output by said discriminator circuit, and said received data signal; and

a clock recovery circuit for being controlled by said first and second feedback loops to output the clock signal recovered;

the clock signal output from said clock recovery circuit being supplied as a clock signal for discrimination by said discriminator circuit.

3. The clock and data recovery circuit according to claim 2, wherein said first feedback loop includes:

a voltage-controlled oscillator circuit for varying the oscillation frequency based on an input control signal voltage;

a first phase detector circuit supplied with a clock signal output from said voltage-controlled oscillator circuit and with said received data signal to detect the phase difference between the two input signals; and

a first integrator circuit for integrating an output of said first phase detector circuit and for supplying an output voltage to said voltage-controlled oscillator circuit as a control signal voltage; and wherein

said second feedback loop includes:

a discriminator circuit supplied with said received data signal;

a second phase detector circuit supplied with an output data signal, output from said discriminator circuit, and with said received data signal, to detect the phase difference between the two signals supplied;

a second integrator circuit for integrating an output of said second phase detector circuit; and

a phase shift circuit receiving said clock signal output from said voltage-controlled oscillator circuit and an integrated output of said second integrator circuit, for shifting the phase of said clock signal in accordance with the integrated output received, to output the resulting clock signal;

said clock signal, output from said phase shift circuit, being supplied to said discriminator circuit as a clock for discrimination and output as an output clock signal.

4. A clock and data recovery circuit comprising:

a first feedback loop including a first phase detector circuit for detecting the phase difference between an input reference clock signal and a recovered clock signal; and

a second feedback loop including a discriminator circuit supplied with a received data signal and a second phase detector circuit for detecting the phase difference between the data signal discriminated and output by said discriminator circuit and said received data signal;

a clock for discrimination of said discriminator circuit being supplied from a clock recovery circuit controlled by said first and second feedback loops.

5. The clock and data recovery circuit according to claim 4, wherein said first feedback loop includes:

a voltage-controlled oscillator circuit for varying the oscillation frequency based on an input control signal voltage;

a first phase detector circuit receiving the clock signal output from said voltage-controlled oscillator circuit and said reference clock signal to detect the phase difference therebetween, and

a first integrator circuit for integrating an output of said first phase detector circuit to supply the resulting output voltage to said voltage-controlled oscillator circuit as a control signal voltage; and wherein

said second feedback loop includes:

a discriminator circuit supplied with said received data signal;

a second phase detector circuit supplied with the data signal output from said discriminator circuit and with said received data signal to detect the phase difference between the two signals supplied;

a second integrator circuit for integrating an output of said second phase detector circuit; and

a phase shift circuit supplied with said clock signal output from said voltage-controlled oscillator circuit and with an integrated output of said second integrator circuit to phase-shift the input clock signal depending on the input integrated output;

the clock signal, output from said phase shift circuit, being supplied to said discriminator circuit as the clock for discrimination, and being output as an output clock signal.

6. The clock and data recovery circuit according to claim 4, wherein said first phase detector circuit includes a selection circuit for selecting said received data signal or said reference clock signal, as a signal to be subjected to phase comparison with said clock signal.

7. The clock and data recovery circuit according to claim 6, wherein said first feedback loop includes:

a selection circuit supplied with a reference clock signal and with said received clock signal to output one of the signals based on a selection control signal;

a voltage-controlled oscillator circuit for varying the oscillation frequency based on an input control signal voltage;

a first phase detector circuit supplied with a clock signal output from said voltage-controlled oscillator circuit and with a signal from said selection circuit to detect the phase difference therebetween; and

a first integrator circuit for integrating an output of said first phase detector circuit to supply the resulting output voltage as a control signal voltage to said voltage-controlled oscillator circuit; and wherein

said second feedback loop includes:

a discriminator circuit supplied with said received data signal;

a second phase detector circuit supplied with an output of said discriminator circuit and with said received data signal to detect the phase difference therebetween;

a second integrator circuit for integrating an output of said second phase detector circuit; and

a phase shift circuit supplied with a clock signal output from said voltage-controlled oscillator circuit and with an integrated output of said second integrator circuit to shift the phase of the input clock signal in accordance with said integrated output supplied to output the

resulting clock signal;

the clock signal output from said phase shift circuit being supplied to said discriminator circuit as a signal for discrimination and being output as an output clock signal.

8. The clock and data recovery circuit according to any one of claims 2 to 7, wherein the time constant of said first feedback loop is selected to be larger than the time constant of said second feedback loop.

9. The clock and data recovery circuit according to any one of claims 3, 5 and 7, wherein the time constant of said first integrator circuit is selected to be larger than the time constant of said second integrator circuit.

10. A clock and data recovery circuit comprising:

a first phase detector circuit for comparing the phase of an input data signal supplied to a first input end thereof with that of a clock signal supplied to a second input end thereof to output a comparison result at an output end thereof;

a first integrator circuit supplied with an output signal from said first phase detector circuit to integrate the signal supplied;

a clock recovery circuit supplied with an output signal of said first integrator circuit at an input end thereof to change the oscillation frequency based on an output signal from said first integrator circuit to output the resulting clock signal at an output end thereof;

said clock signal, output from said clock recovery circuit, being fed back to a second input end of said first phase detector circuit;

a discriminator circuit supplied with said input data signal at a data input end thereof to discriminate said input data signal based on a clock signal for discrimination supplied to a clock input terminal thereof to output a data signal at an output end thereof;

a second phase detector circuit for comparing the phase of the data signal supplied to a first input end thereof from said discriminator circuit with that of said input data signal supplied to a second input end thereof to output a comparison result at an output end thereof;

a second integrator circuit supplied with an output signal from said second phase detector circuit to integrate the signal supplied; and

a phase shift circuit supplied with said clock signal output from said clock recovery circuit at an input end thereof and with an output signal from said second integrator circuit at a control signal input end thereof to shift the phase of the clock signal output from said clock recovery circuit, based on said output signal, to output the resulting clock signal at an output end thereof;

the clock signal output from said phase shift circuit being supplied to said discriminator circuit as said clock signal for discrimination.

11. A clock and data recovery circuit including a discriminator circuit for discriminating an input data signal responsive to a clock signal for discrimination to output an output data signal, and a clock generating circuit supplied with said input data signal or with a reference clock signal to generate a clock signal synchronized with the signal supplied;

said clock and data recovery circuit comprising:

a feedback loop for detecting the phase difference between said output data signal and said signal supplied, and for shifting the phase of said clock signal based on the result of integration of said phase difference to supply the resulting clock signal to said discriminator circuit as said clock signal for discrimination.